Serial Front Panel Data Port is an industry standard, low-overhead, low-latency, high speed serial communications protocol. sFPDP is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. The simple and lightweight nature of the protocol makes it an attractive choice for replacement of parallel bus interconnects using serial transceiver technology. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient and flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver based devices from Altera and Xilinx as well as Microsemi Igloo-2 devices. We’re always making improvements to the core with innovative new features such as multi-lane bonding for increased bandwidth, and we’re continually updating the core to support new transceiver based devices offered by Altera, Xilinx, and Microsemi. Our core provides a open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench with support for Aldec's Active-HDL and Riviera-Pro as well as Mentor's ModelSim tools. In addition, our testing procedure includes exhaustive interoperability testing among all FPGA families and manufacturers to ensure compatibility.

StreamDSP is committed to delivering the highest level of customer support to ensure smooth system integrations. We also offer IP core customization and FPGA design services.
Resource Usage

<table>
<thead>
<tr>
<th>Registers</th>
<th>LUTs</th>
<th>*RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>772</td>
<td>841</td>
<td>14 Blocks</td>
</tr>
</tbody>
</table>

* RAM size dependent on user controlled TX and RX FIFO depths

Throughput (per lane)

<table>
<thead>
<tr>
<th>Line Rate</th>
<th>Throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 Gbps</td>
<td>247 MB/s</td>
</tr>
<tr>
<td>4.25 Gbps</td>
<td>420 MB/s</td>
</tr>
<tr>
<td>5.0 Gbps</td>
<td>494 MB/s</td>
</tr>
<tr>
<td>6.375 Gbps</td>
<td>630 MB/s</td>
</tr>
<tr>
<td>8.5 Gbps</td>
<td>841 MB/s</td>
</tr>
<tr>
<td>10.0 Gbps</td>
<td>990 MB/s</td>
</tr>
</tbody>
</table>

Delivery Options

HDL Language: VHDL
License Types:
- Netlist
- Source Code

* Free, supported evaluations available on request
# FPGA Family Support

## ALTERA/INTEL
- **Cyclone-IV GX**: Altera Cyclone-IV GX Starter Kit
- **Cyclone-V GX/SX**: Arrow Cyclone-V SoCkit
- **Cyclone-10 GX**: Intel Cyclone-10 GX Development Kit
- **Arria GX**: Altera Arria-GX PCIe Dev Kit
- **Arria-II GX**: Altera Arria-II GX PCIe Dev Kit
- **Arria-II GZ**: Full working TB and example designs
- **Arria-V GX**: Altera Arria-V GX Starter Kit
- **Arria-V GZ**: Full working TB and example designs
- **Arria-10 GX**: Altera Arria-10 Development Board
- **Stratix-II GX**: Altera Stratix-II GX PCIe Dev Kit
- **Stratix-IV GX**: Altera Stratix-IV GX PCIe Dev Kit
- **Stratix-V GX**: Altera Stratix-V GX PCIe Dev Kit
- **Stratix 10**: Altera Stratix-10 FPGA Development Kit

## XILINX
- **Virtex-2 Pro**: Custom Hardware board
- **Spartan-6 LXT**: Xilinx SP605 Development Kit
- **Kintex-7**: Xilinx KC705 Evaluation Kit
- **Virtex-4 FX**: Xilinx ML405 Development Kit
- **Virtex-5 LXT**: Xilinx ML555 Development Kit
- **Virtex-5 FXT**: Xilinx ML507 Development Kit
- **Virtex-6 LXT**: Xilinx ML605 Development Kit
- **Virtex-7 GTX**: Xilinx VC707 Evaluation Kit
- **Virtex-7 GTH**: Xilinx VC709 Evaluation Kit
- **Artix-7**: Xilinx AC701 Development Kit
- **Kintex-UltraScale**: Xilinx KCU105 Development Kit
- **Virtex-UltraScale**: Xilinx VCU108 Development Kit
- **Zynq-7000 GTX**: Xilinx ZC706 Development Kit
- **Zynq-7000 GTP**: Custom Board
- **Virtex-UltraScale+**: Xilinx VCU118 Development Kit
- **Zynq-UltraScale+ GTH**: Xilinx ZCU102 Development Kit (MPSoC)
- **Zynq-UltraScale+ GTY**: Xilinx ZCU111 Development Kit (RFSoC)

## MICROSEMI
- **Igloo-2**: Microsemi Igloo-2 Evaluation Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).