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IP Datasheet

Interlaken-PHY

for Altera and Xilinx FPGAs

Interlaken is a royalty-free interconnect protocol that was developed by Cisco Systems and Cortina Systems in 2006. The full Interlaken protocol (described in the Interlaken Protocol Specification, v1.2) was designed to support chip-to-chip packet transfers in high-bandwidth networking equipment. A full Interlaken solution consists of the Interlaken **Protocol Layer** which runs on top of the Interlaken **Framing Layer**. The full Interlaken protocol is often viewed as too complex for designers who are looking for a lightweight, low-overhead way to connect multiple FPGAs, systems, or sensors. For these cases, the Interlaken **Framing Layer** gives us everything we need for an extremely scalable, high-bandwidth, low-overhead and lightweight FPGA interconnect that **supports any FPGA device family** all with a common user interface. The Interlaken **Framing Layer** is combined with the FPGA transceiver to form a complete IP core that we call the **StreamDSP Interlaken-PHY IP Core**.

It's important to note that the Interlaken-PHY IP core is **NOT** a full Interlaken Protocol implementation because it only implements the Framing Layer of the Interlaken specification. The Interlaken-PHY IP Core gives users an extremely easy and efficient way to achieve scalable, high-bandwidth, low overhead connections between FPGAs, systems, and sensors. The Interlaken-PHY IP Core provides a simple, parallel, streaming data interface to the user and does not support data packetization, virtual channels, framing, flow control, or other features found in full-featured protocols. The user interfaces with customizable-depth FIFOs on the input and output of the core. On the transmit side, the user is responsible for not allowing the TX FIFO to empty by writing data to it at a rate greater than or equal to (Line_Rate/67). If there is no data to send, the controlIn input bit can be used to write “Empty” control words which can then be ignored at the destination. On the receive side, the user is responsible for not allowing the RX FIFO to overflow by reading it at a fast enough rate which also defined as greater than or equal to (Line_Rate/67). For example, if the Line_Rate of the FPGA transceiver(s) is 10.0 Gbps then the user interface clock must be greater than or equal to 149.26 MHz. For a more detailed explanation of the user interface, please see the complete StreamDSP Interlaken-PHY User Guide.

StreamDSP is committed to performance, efficiency, and flexibility, and we’re continually updating the core to support new transceiver based devices offered by both Altera and Xilinx. A complete reference design is provided for each family, as well as a self-verifying testbench. In addition, our testing procedure includes exhaustive Altera <-> Xilinx interoperability testing to ensure compatibility.

StreamDSP is committed to delivering the highest level of customer support to ensure a smooth system integration. We also offer IP core customization and FPGA design services.

Features

- ☑ Fully compliant with Interlaken Protocol v1.2 Framing Layer specification
- ☑ Any number of physical lanes supported
- ☑ Channel bonding handled by core
- ☑ Runs at any rate supported by transceiver
- ☑ User datapath width of 64-bits per lane
- ☑ Automatic, self-synchronizing link(s)
- ☑ Support for Altera and Xilinx FPGAs
- ☑ 64B/67B Data Encoding
- ☑ Over 95% Bandwidth efficient
- ☑ Ensures DC balance by bounding baseline wander for high link stability
- ☑ 58-bit Synchronous Scrambler
- ☑ Guarantees bit transitions
- ☑ Ensures low EMI characteristics
- ☑ Allows link to self-synchronize without user intervention
- ☑ CRC32 generation and verification
- ☑ Verifies data integrity
- ☑ Identifies lane(s) with data errors

Uses

- ☑ Low overhead, scalable interconnects
- ☑ Excellent choice for streaming sensor data
- ☑ High-bandwidth backplanes
- ☑ High-bandwidth cables
- ☑ Many users choose to build their own custom protocol on top of this Interlaken-PHY

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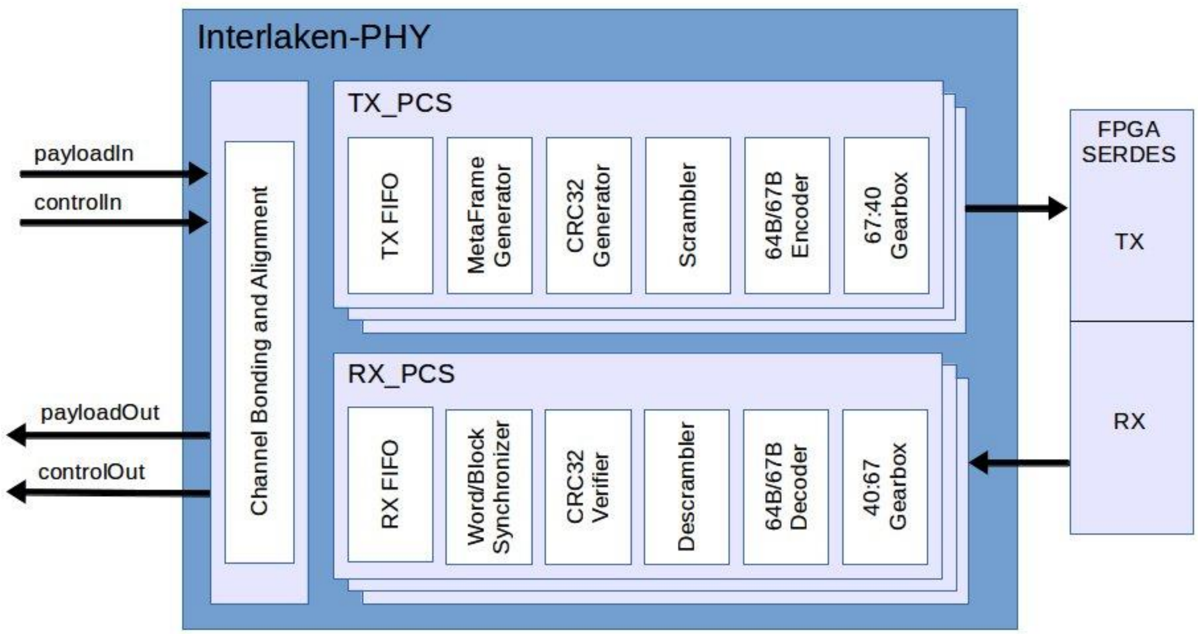
Details



Resource Usage

Registers	LUTs	RAM
1803	1891	4 Blocks

* single-lane application. Resources scale linearly with number of lanes

Throughput Examples

1 lane @ 2.5 Gbps = 296 MB/s
4 lanes @ 5.0 Gbps = 2375 MB/s
10 lanes @ 14.1 Gbps = 16,743 MB/s

Delivery Options

HDL Language: **Verilog**
License Types:

- Netlist
- Source Code

* Free, supported evaluations available on request

FPGA Family Support

ALTERA/INTEL	Example Design
• Stratix-IV GX	Altera Stratix-IV GX PCIe Dev Kit
• Stratix-V GX	Altera Stratix-V GX PCIe Dev Kit
• Arria-V GX	Altera Arria-V GX PCIe Dev Kit
• Arria-10 GX	Altera Arria-10 GX PCIe Dev Kit
• Stratix-10 GX L-Tile	Intel Stratix-10 GX PCIe L-Tile Dev Kit
• Stratix-10 GX H-Tile	Intel Stratix-10 GX PCIe H-Tile Dev Kit
XILINX	
• Kintex-7	Xilinx KC705 Evaluation Kit
• Artix-7	Xilinx AC701 Evaluation Kit
• Virtex-6 GTX	Xilinx ML605 Evaluation Kit
• Virtex-7 GTX	Xilinx VC707 Evaluation Kit
• Virtex-7 GTH	Xilinx VC709 Evaluation Kit
• Kintex UltraScale	Xilinx KCU105 Evaluation Kit
• Virtex UltraScale	Xilinx VCU108 Evaluation Kit
• Virtex UltraScale+	Xilinx VCU118 Evaluation Kit
• Zynq UltraScale+	Xilinx ZCU102 Evaluation Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).